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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
CHANG, AUDREY Y	
ART UNIT	PAPER NUMBER
2872	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/630,883	GOLSHAN, KHOSROW	
	Examiner	Art Unit	
	Audrey Y. Chang	2872	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 March 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *47-78* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *47-78* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on March 21, 2008 has been entered.

2. This Office Action is also in response to applicant's amendment filed on January 22, 2008, which has been entered into the file.

3. By this amendment, the applicant has amended claims 47, 55, 65, and 69.

4. Claims 47-78 remain pending in this application.

5. The objection the drawing set forth in the previous Office Action are withdrawn.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. **Claims 47-58 and 63-78 are rejected under 35 U.S.C. 103(a) as being unpatentable over the patent issued to Yang et al (PN. 5,239,173) in view of the patent issued to Stotts et al (PN. 4,128,300), Usagawa et al (PN. 5,233,205).**

Yang et al teaches *binary data processor* that is comprised of a plurality of optical pathways defined by waveguides (41 and 42, Figure 5), wherein the plurality of optical pathways forming an optical logic gate having a first input and a second input (13 and 14, Figure 5) for receiving coherent light beam

from a coherent light source (11). The optical waveguides or the plurality of optical pathways are formed with a shutter (15 and 16) so that it could be selectively switched ON or OFF. The binary data processor further comprises an interference region that is formed by material, served as the second material, wherein the interference regions if bounded on all sides excepted where the optical inputs and optical output are located, by a wall material (18), wherein the wall material is other than the second material. The interference region implicitly has to be three dimensional region that contains no potential barrier portioning the interference region.

The optical inputs (13 and 14) are spaced apart and the optical output is positioned along a chosen line along, (please see Figure 5). With regard to the feature concerning "*the output is positioned along a chosen line along which destructive interference occurs*". Yang et al does not teach such explicitly however this feature is to the least inherently met by the cited reference **since** the optical logic gate of Yang et al *performs the same Boolean logic functions* as the instant application and the output signal of the Boolean logic function is the *direct result of the interference* of the input optical signals, the arrangement of the output therefore has to align in the claimed manner to produce the Boolean logic output results. With regard to the feature of the "interference line is aligned with the output when the light input at the second input is on". This feature is implicitly included in the disclosure since only when light propagates through the pathways, the interference of light waves occur. It is implicitly true that within the interference region there is at least one axis along which maximum constructive interference would occur.

Yang et al teaches that a optical output signal may be a Boolean logic output signal wherein the Boolean logic includes "NOT" or inversion logic function, (please see column 3, lines 35-39, column 4, lines 4-5).

This reference has met all the limitations of the claims. It however does not teach explicitly that the waveguides or the plurality of pathways are formed of the same material as the interference region

and the second material are overlaying on a substrate of a first material. Stotts et al in the same field of endeavor teaches an structure of an optical logic element, wherein the plurality of pathways (12, 13, 15, 16, and 17, Figure 1) or the waveguide and interference region (14, Figure 1), are made of same waveguide material. Usagawa et al in the same field of endeavor teaches an optical logic element wherein optical pathway and interference regions can be formed by patterning an optical layer (52, Figure 5B) and makes it overlaying a substrate material (50), with the optical layer bounded by a third material on all sides of it. It would then have been obvious to one skilled in the art to apply the teachings of **Stotts** et al and **Usagawa** et al to make the binary data processor that performs Boolean logic function with patterned optical layer for the plurality of pathways and interference region that overlying on a substrate material for the benefit of using standard waveguide material and structure to facilitate the binary data processor.

With regard to the feature that the "output signal having one of two intensities, either a substantially on or a substantially off intensity". This feature is implicitly met by the disclosure of Yang et al et al, since Yang et al et al teaches a *Boolean logic gate and* the optical output signal is a *Boolean logic output signal,* which implicitly include ON and OFF output intensities.

With regard to claims 48, 51, 56-58, 66, 70-72, and 74, both Yang et al and Usagawa et al references teach the optical logic circuit may be designed to give NOT logic function as the output signal. Yang et al teaches that the NOT operation requires interference of signal beam and reference beam and being observed at a cancellation angle, (please see column 3, line 63 to column 4 line 8). Usagawa et al teaches (Figure 1D), an optical input signal may be a *constant coherent input signal*, ("1") that enters the interference regions through the input gate (10), and a *second input coherent optical signal* (X) may be switched ON or OFF and enters the interference region through the *second input gate* (10'). When the second coherent input signal is turned ON, the input signals from both gates interfere with each other to

essentially cancel each other so that an invert or NOT optical logical function is resulted as the optical output signal, (please see Figure 1D, column 8, lines 8-25).

With regard to claims 49-50, 67, 68, 69, 75, and 77, Usagawa et al teaches that the optical logic circuit may be designed to give NAND logic function, (Figure 1F), wherein three input optical signals are used. One skilled in the art certainly can design the optical processor to comprise various logic gates for the desired logical functions and purposes.

It is not clear how the third optical input is related to the first and second optical inputs, this feature can only examined in the broadest interpretation. Usagawa et al teaches that specific optical gate can be formed using three optical inputs, as shown in Figure 1B and 1C.

With regard to claims 63 and 64, this reference also does not teach explicitly that a laser diode or a semiconductor diode is used as the light source for generating the optical wave. However laser diode or laser semi-conductive diode are both well known light sources for operating optical logic circuit, such feature is either inherently met or an obvious modification to one skilled in the art for providing proper light sources with proper energy required to operate the optical logic circuit.

With regard to claim 69, it is implicitly true that the interference properties of the input signals in the interference region are determined by the input signals and the physical structure of the interference region.

8. **Claims 59-62 are rejected under 35 U.S.C. 103(a) as being unpatentable over the patent issued to Yang et al, Stotts et al and Usagawa et al as applied to claim 55 above, and further in view of the patent issued to Logan et al (PN. 3,837,728).**

The optical logic circuit taught by **Yang et al in combinations of Stotts et al and Usagawa** et al as described for claim 55 above has met all the limitations of the claims. Yang et al does not teach explicitly about the materials used for making the binary data processor. **Usagawa** et al teaches that the

optical logic circuit may use gallium arsenide (GaAs) material as the substrate layer however it does not teach explicitly to use doped GaAs material, silicon or doped silicon materials as the substrate layer and optical layer for pathways (i.e. waveguides) respectively. But these materials are all well known semi-conductive materials for making waveguides or even optical logic circuit, as demonstrated by the teachings of *Logan* et al wherein a GaAs layer is used as substrate layer wherein doped GaAs layer is used as the optical waveguide. It would then have been obvious matters of design choices to one skilled in the art to use the claimed materials as the materials for designing the optical logic circuits for the benefit of using desired materials that provide the desired performance. It has also been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended used as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

9. **Claims 47-58 and 63-78 are rejected under 35 U.S.C. 103(a) as being unpatentable over the patent issued to Stotts et al (PN. 4,128,300) in view of the patent issued to Usagawa et al (PN. 5,233,205).**

Stotts et al teaches an *optical logic element* wherein the optical logic element comprises a plurality of *optical waveguides or optical pathways* forming a plurality of optical logic gates wherein at least some of the optical logic gates having a first and second inputs for receiving coherent light input from a light source and an *interference region* coupled to the first and second inputs, (please see coupler region 14, having an interference region coupled to the first and second input). Stotts et al teaches that the optical logic element is capable of providing Boolean logic output signal based on the output signal from the interference region, wherein the optical logic element can be designed to provide **NOT, NOT AND (NAND) and exclusive OR (NOR) optical logic functions, respectively**, (please see column 2 line 56 to column 3, line 12, Figures 2 and 3). **Stotts** et al teaches that the light propagation through the first and second input can be controlled via photoconductive path (18 and 19) so that when the light

source is ON the interference between the light propagated via the first and second wave guides or inputs can produce *destructive* interference and output waveguide is placed along the lines of destructive interference occurrence to provide the desired logic function, (please see column 5, line 65 to column 6, line 5).

Stotts et al teaches that the optical logic element comprises a substrate (10, Figure 1), which essentially is comprised of a first material for supporting the various optical waveguides. This reference however does not teach explicitly that the optical wave guides are formed within an optical layer overlaying the substrate and comprised of a second material. Usagawa et al in the same field of endeavor teaches an optical logic circuit having plurality of waveguides or optical pathways and interference region wherein the logic circuit is formed by transparent material such as GaAs, (52, Figure 5B or 100, 101, 102 in Figure 6B) that is overlying a substrate (50 Figure 5B and 91) that is bounded by other material (such as $Al_xGa_{1-x}As$) on all sides of the material for making the optical paths and interference region.
In would then have been obvious to one skilled in the art to apply the teachings of Usagawa et al actually manufactures the optical logic element.

With regard to the feature that the "output signal having one of two intensities, either a substantially on or a substantially off intensity". This feature is implicitly met by the disclosure of Stotts et al, since Stotts et al teaches a *Boolean logic gate and* the optical output signal is a *Boolean logic output signal,* which implicitly include ON and OFF output intensities.

With regard to the feature that the interference of the waves are caused exclusive by the interactions of the input waves, such is implicitly included since interference between waves can only be caused by the interactions of the waves.

With regard to claim 69, it is implicitly true that the interference properties of the input signals in the interference region are determined by the input signals and the physical structure of the interference region.

With regard to claims 63 and 64, this reference also does not teach explicitly that a laser diode or a semiconductor diode is used as the light source for generating the optical wave. However laser diode or laser semi-conductive diode are both well known light sources for operating optical logic circuit, such feature is either inherently met or an obvious modification to one skilled in the art for providing proper light sources with proper energy required to operate the optical logic circuit.

10. **Claims 59-62 are rejected under 35 U.S.C. 103(a) as being unpatentable over the patent issued to Stotts et al and Usagawa et al as applied to claim 55 above, and further in view of the patent issued to Logan et al (PN. 3,837,728).**

The optical logic circuit taught by **Stotts** et al as in combination with the teachings of **Usagawa** et al described for claim 55 above have met all the limitations of the claims. Usagawa et al teaches that the optical logic element may use GaAs material as the substrate layer however it does not teach explicitly to use doped GaAs material, silicon or doped silicon materials as the substrate layer and optical layer for pathways (i.e. waveguides) respectively. But these materials are all well known semi-conductive materials for making waveguides or even optical logic circuit, as demonstrated by the teachings of Logan et al wherein a GaAs layer is used as substrate layer wherein *doped* GaAs layer is used as the optical waveguide. It would then have been obvious matters of design choices to one skilled in the art to use the claimed materials as the materials for designing the optical logic circuits for the benefit of using desired materials that provide the desired performance. It has also been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended used as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Response to Arguments

11. Applicant's arguments filed on January 22, 2008 have been fully considered but they are not persuasive. The newly amended claims have been fully considered and they are rejected for the reasons stated above.

12. The applicant is respectfully noted that the cited Stotts et al reference does teach explicitly that there is no potential barriers present in the interference region (14, Figure 1). Applicant's arguments concerning barrier for separating the input waveguides are wrong since this barrier is not in the interference region. Furthermore, by applicant's arguments the instant application as shown in Figure 8 also has potential barrier for separating pathways which makes the statement "*interference region ... contains no potential barriers partitioning the interference region*" recited in claims 47, 55, 65, and 69 a wrong statement.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Audrey Y. Chang whose telephone number is 571-272-2309. The examiner can normally be reached on Monday-Friday (9:00-4:30), alternative Mondays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephone B. Allen can be reached on 571-272-2434. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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